IN THE CLAIMS

Please cancel non-elected claim 17-29 without prejudice. Please amend claims 3-4, 8-10, and 12-16. Please also add claims 30-44.

1. (Original) A semiconductor device comprising:

a semiconductor body having a top surface and laterally opposite sidewalls formed on a substrate;

a gate dielectric formed on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

a film formed adjacent to said semiconductor body wherein said film produces a stress in said semiconductor body.

2. (Original) The semiconductor device of claim 1 wherein said film produces a compressive stress in said semiconductor body.

3. (Amended) The semiconductor device of claim 1 wherein said film produces a ~~tinsel~~ tensile stress in said semiconductor body.

4. (Amended) The semiconductor device of claim 1 wherein said film has ~~tinsel~~ tensile stress.

5. (Original) The semiconductor device of claim 1 wherein said film has a compressive stress.

6. (Original) The semiconductor device of claim 5 wherein said compressive film comprises silicon nitride.

7. (Original) The semiconductor device of claim 1 wherein said semiconductor body is a single crystalline silicon film.

8. (Amended) The semiconductor device of claim 1 wherein said semiconductor body is selected from the group consisting of silicon, germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

9. (Amended) A ~~tri-gate transistor~~ semiconductor device comprising:

a single crystalline silicon body formed on insulating substrate, said silicon body having a top surface opposite a bottom surface and a first and second laterally opposite sidewalls;

a gate dielectric formed on said top surface of said semiconductor body and on said first and second laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric and on said top surface of said silicon body and adjacent to said gate dielectric on said first and second laterally opposite sidewalls of said silicon body;

a pair of source/drain regions formed in said silicon body on opposite sides of said gate electrode; and

a stress induced film formed around said silicon body and said gate electrode, said film providing stress in the channel region of said device.

10. (Amended) The ~~method~~ semiconductor device of claim 9 wherein said thin film has a compressive stress and places a ~~tinsel~~ tensile stress in said channel region.

11. (Original) The semiconductor device of claim 10 wherein said thin film comprises a silicon nitride film.

12. (Amended) The semiconductor device of claim 9 wherein said thin film has ~~tinsel~~ tensile stress and incorporates a compressive stress into said channel region of said semiconductor body.

13. (Amended) The ~~tri-gate transistor~~ semiconductor device of claim 10 wherein said semiconductor body channel region is doped to a p type conductivity with a concentration level between $1x10^{16} - 1x10^{19}$ atoms/cm^3.

14. (Amended) The ~~tri-gate~~ semiconductor device of claim 12 wherein said channel region of said semiconductor body is doped to a n type conductivity with a concentration level between $1x10^{16} - 1x10^{19}$ atoms/cm^3.

15. (Amended) The ~~tri-gate transistor~~ semiconductor device of claim 9 wherein said thin film completely surrounds said semiconductor body and said gate electrode.

16. (Amended) The ~~method~~ semiconductor device of claim 9 wherein a thin grown oxide layer is formed between the bottom of said semiconductor body and said thin film.

17 – 29 (Withdrawn)

30. (New) A semiconductor device comprising:

a semiconductor body having a top surface opposite a bottom surface and laterally opposite sidewalls;

a gate dielectric disposed on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode disposed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

a first film disposed subjacent to the bottom surface of said semiconductor body, said first film to produce stress in said semiconductor body.

31. (New) The semiconductor device of claim 30, wherein at least a portion of said bottom surface is a passivated bottom surface.

32. (New) The semiconductor device of claim 30, wherein a second film is disposed between a portion of the bottom surface of said semiconductor body and said first film.

33. (New) The semiconductor device of claim 30, wherein said second film comprises oxide.

34. (New) The semiconductor device of claim 30, wherein said first film comprises silicon nitride.

35. (New) A semiconductor device comprising:

a semiconductor body having a top surface opposite a bottom surface and laterally opposite sidewalls;

a gate dielectric disposed on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode disposed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

a continuous film disposed superjacent to at least a portion of the gate electrode and a portion of the top surface of said semiconductor body, adjacent to at least a portion of the gate electrode and a portion of the sidewalls of said semiconductor body, and subjacent to at least a portion of the bottom surface of said semiconductor body, said film to produce stress in said semiconductor body.

36. (New) The semiconductor device of claim 35 wherein said continuous film has tensile stress.

37. (New) The semiconductor device of claim 35 wherein said continuous film has compressive stress.

38. (New) A semiconductor device comprising:

a semiconductor body formed on insulating substrate, said semiconductor body having a top surface opposite a bottom surface and a first and second laterally opposite sidewalls;

a gate dielectric formed on said top surface of said semiconductor body and on said first and second laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric and on said top surface of said semiconductor body and adjacent to said gate dielectric on said first and second laterally opposite sidewalls of said semiconductor body;

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode;

a first film disposed on the source/drain regions, said first film comprising a semiconductor; and

a second film formed adjacent to said semiconductor body, said second film providing stress in said semiconductor body.

39. (New) The semiconductor device of claim 38 wherein said first film is selected from a group consisting of silicon, silicon germanium, silicide, titanium silicide, nickel silicide, and cobalt silicide

40. (New) The tri-gate transistor of claim 39 wherein said first film is electrically isolated from said gate electrode.

41. (New) The tri-gate transistor of claim 38, further comprising a third film disposed on the first film, said third film comprising silicide.

42. (New) A semiconductor device comprising:

a semiconductor body having a top surface and laterally opposite sidewalls formed on a substrate;

a gate dielectric formed on said top surface of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body; and

a dielectric film formed adjacent to the semiconductor body, said film to produce a stress in the semiconductor body.

43. (New) The semiconductor device of claim 41 wherein said dielectric film to produce a tensile stress in said semiconductor body.

44. (New) The semiconductor device of claim 41 wherein said dielectric film to produce a compressive stress in said semiconductor body.